

# First Demonstration of Correlation in a Niobium Superconductive Programmable Binary-Analog Matched Filter

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**Abstract**—A complete prototype superconductive programmable binary-analog matched filter for a 2-Gchip/s spread-spectrum modem has been operated for the first time and has performed correlation. We had previously demonstrated functionality of each individual element of the filter. The analog samplers had captured signals with bandwidths in the order of 10 GHz; the binary-weighted taps, which utilize the unique quantum mechanical properties of superconductive circuits, had exhibited nondestructive readout as required; and the two digital shift registers, one that stores the binary code pattern and one that controls sampling of the input analog signal in the bank of track-hold cells, had functioned at 2 GHz. Now all of these elements have been operated together in low-frequency tests. A 7-bit (or “chip” in spread-spectrum terminology) pseudo-noise (pn) code sequence was loaded into the reference shift register in each of the seven possible positions while an analog version of the pn code with its amplitude varied over the full bipolar dynamic range of the filter was used as the incoming signal. The filter response peaked as expected when the analog signal and the binary reference were aligned. The peak and sidelobe responses agreed quantitatively with those predicted from calibration measurements made with uniform signals instead of pn codes.

## I. INTRODUCTION

At the Applied Superconductivity Conference (ASC) in 1992 [1] we described a high-speed superconductive analog sampler, which we call the Davidson sampler, intended at the time for application in a wideband, single-shot waveform recorder. Experimental results showing sampling of a 500 MHz signal were presented. At the 1993 Government Microcircuit Applications Conference (GOMAC) [2] and at the 1994 ASC [3] we presented the architecture of a direct-sequence spread-spectrum modem intended to operate at a data rate of 2-gigachips-per-second (“chip” is the spread-spectrum term for a bit in the high-speed spreading code as distinguished from a bit in the lower-speed signal that is being spread). We described the operation of the individual subcircuits in the analog-binary programmable matched filter for such a modem. The analog modules include analog samplers and track/hold (T/H) circuits and a nondestructive-readout (NDRO) binary-weighted analog tap circuit. We presented experimental results in which the Davidson sampler accurately captured a pulse waveform with a rise time of about 250 ps, and we showed how the same circuit—but with a very low L/C product—could use the quantum

mechanics of flux quantization to perform the NDRO operation.

At the 1996 ASC [4] operation of the digital circuits in the filter was described. A Modified Variable Threshold Logic (MVTL) OR gate was fully characterized, both as an isolated gate and when driving other gates as in the filter’s digital shift registers. An interface buffer circuit that could amplify the output levels from MVTL digital gates to the higher voltages and currents needed to drive the analog modules was also characterized. Preliminary experiments that indicated successful operation of a seven-stage shift register were presented for clock frequencies up to 1 GHz. At the 1997 ISEC conference [5], full operation of the shift registers at 2 GHz was reported. Since no proceedings paper was published from that conference, one of those results is included here in Fig. 5.

In this paper we present the first experimental results in which an entire prototype filter was operated. This test filter, containing registers with seven stages, successfully performed correlations using a 7-chip pseudo-noise (pn) sequence.

## II. PROGRAMMABLE FILTER OVERVIEW

The modem’s receiver channel requires a programmable matched filter (correlator) for establishing time synchronization between the receiver and the transmitter and for demodulating (despreading) the transmitted signal. A block diagram of the filter is shown in Fig. 1.

The upper section of the diagram shows a pair of digital shift registers with buffered outputs going to the analog components in the lower part of the diagram. The bank of

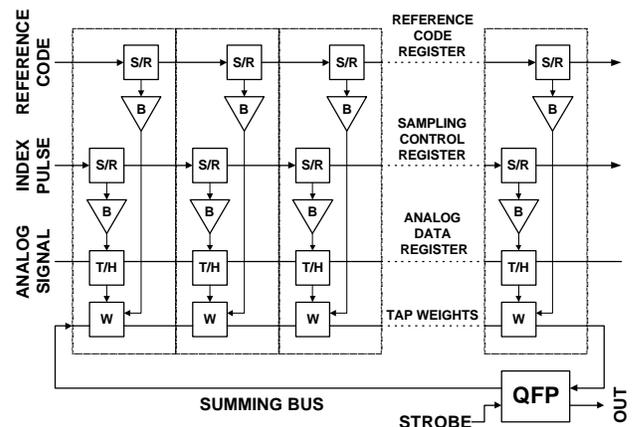


Fig. 1. Block diagram of the superconductive programmable matched filter.

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analog T/H cells (the analog data register) is controlled by the sampling control shift register, which is loaded with all 0's except for a single 1 (the index). The analog input signal is presented to all of the T/H cells, but only where the sampling control register contains a 1 does the corresponding T/H cell capture a new sample; the other cells continue to hold the sample they acquired previously. This 1 circulates through the shift register, causing successive analog samples to be taken in successive T/H cells. Thus, at any given time the most recent N samples of the input signal are stored in the analog data register, with the newest sample at the position of the index, with progressively older samples to the left and then wrapping around to the right, and with the oldest sample just to the right of the index. Note that the signal samples do not move through the analog data register. Rather, each sample remains in place for N clock cycles, at which point it is replaced by a newer sample.

The bank of tap-weight cells is controlled by the binary reference shift register, which is loaded with a time-reversed copy of the code that was used in the transmitter to spread the signal. Each tap multiplies the analog sample stored in the corresponding T/H cell by either +1 or 0 (or, alternatively, +1 or -1) depending on the bit stored in the binary reference register. As the two shift registers are clocked synchronously, the reference code moves past the stationary analog samples of the input signal. When the reference code aligns with the received signal, a correlation peak occurs. The output signal peaks strongly in a positive direction for an encoded signal bit of 1 and in a negative direction for a signal bit of 0. The position in time of the correlation peaks provides synchronization information, while the polarity of each output peak provides the demodulated data bit. Note that in the course of operation, the signal stored in a T/H cell, which, as noted, changes only every N clock cycles, is multiplied by a sequence of varying reference bits. Consequently, the tap-weighting process must be nondestructive; that is, it must not alter the stored analog samples.

For each chip of the spreading code, the filter contains an identical section called a slice, a block diagram of which is shown in Fig. 2(a). The slices are arranged as shown in Fig. 2(b) so that an inductive summing loop can couple to all of the tap elements with a minimum of stray inductance. For the same reason, the slice is kept very narrow, with the OR gates of the three-phase shift registers and the buffer stacked vertically. The output of the buffer in the sampling control register drives the T/H, which is directly below it. The buffer from the binary reference register has to snake by the other circuitry to reach the control input to the tap circuit.

### III. INTEGRATED CIRCUIT LAYOUT

Because the complete prototype filter is too large and complex to show with useful resolution in a single figure, we focus on two subsections. Fig. 3 is a plot from the layout software that shows the top part of the filter, which includes

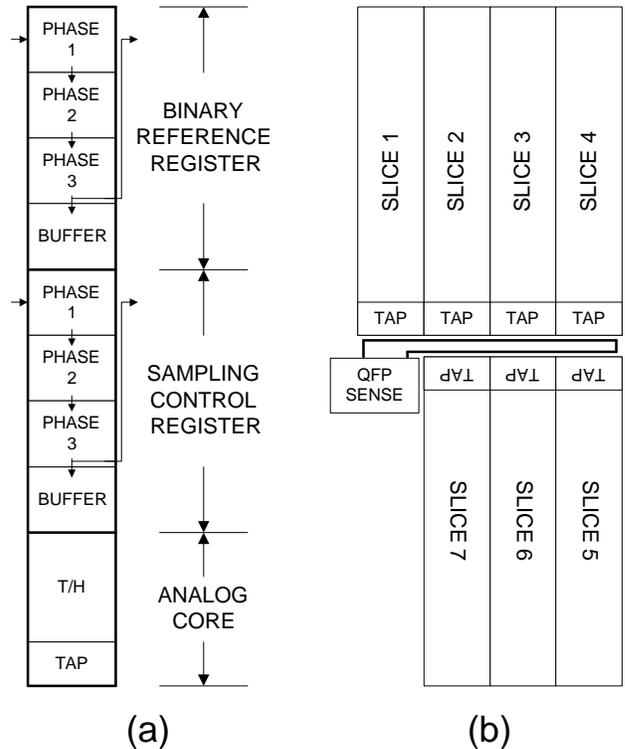


Fig. 2. The filter comprises mainly an array of identical elements, one for each bit in the spreading code. A block diagram of this element, referred to as a slice, is shown in (a). The arrangement of slices to form a seven-stage filter is shown in (b). A wire that runs by and couples inductively to each tap serves as a summing bus, whose signal is connected to a quantum flux parametron (QFP) sense circuit.

the first four stages of the binary reference register. Fig. 4 shows a plot of the analog core section of all seven stages plus the summing bus and the quantum flux parametron (QFP) output comparator. To reduce clutter only three layers are shown: M2 (base-electrode metal), M4 (wiring metal), and R1 (resistors). The circuit layers not shown are M3 (counter-electrode), M5 (ground-plane metal), I2 (vias through the oxide between M2 and M4), and I3 (vias through the oxide between M4 and M5).

### IV. HIGH SPEED OPERATION OF SHIFT REGISTERS

The two shift registers of the prototype filter were operated simultaneously with high-speed waveforms of the type that would be used in full operation of a filter. A 1-GHz word generator with return-to-zero (RZ) outputs was used for the experiment. A 2-GHz non-return-to-zero (NRZ) waveform was produced by combining two channels with a 500 ps phase shift between them. The two channels were programmed with alternating chips of a 15-chip pn code so that, when combined, they produced an NRZ version of the code. (A code with 15 chips rather than 7 was chosen because it has a more varied pattern, including runs of one, two, and three 1s and 0s.) Fig. 5 shows the waveforms captured during the experiment. Since the time delay between the

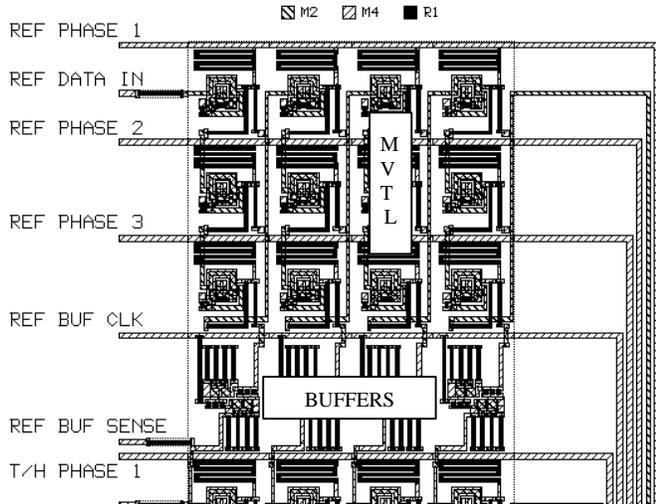


Fig. 3 Layout of the top part of the prototype test filter, showing the three-phase MVTL shift register and buffer array that comprise the binary reference register.

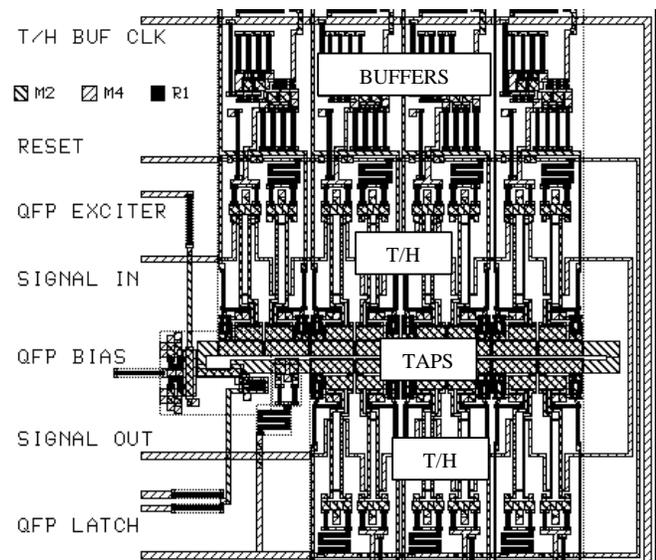


Fig. 4. Layout of the analog core section of the prototype filter. At the top one sees the buffers at the outputs from the sampling control register. The T/H elements, with the input signal applied, are seen above and below the taps, which couple to the summing bus connected to the QFP sense comparator.

input and output signals is largely determined by the lengths of the cables to the oscilloscope; in the figure we have adjusted the timing of the output waveform to align it with the input waveform for easy visual comparison.

## V. OPERATION OF THE PROTOTYPE FILTER

The entire seven-stage prototype filter has been operated for the first time as a filter and has demonstrated matched-filter correlation using a 7-chip pn code sequence, thereby establishing the soundness of the design principles. The

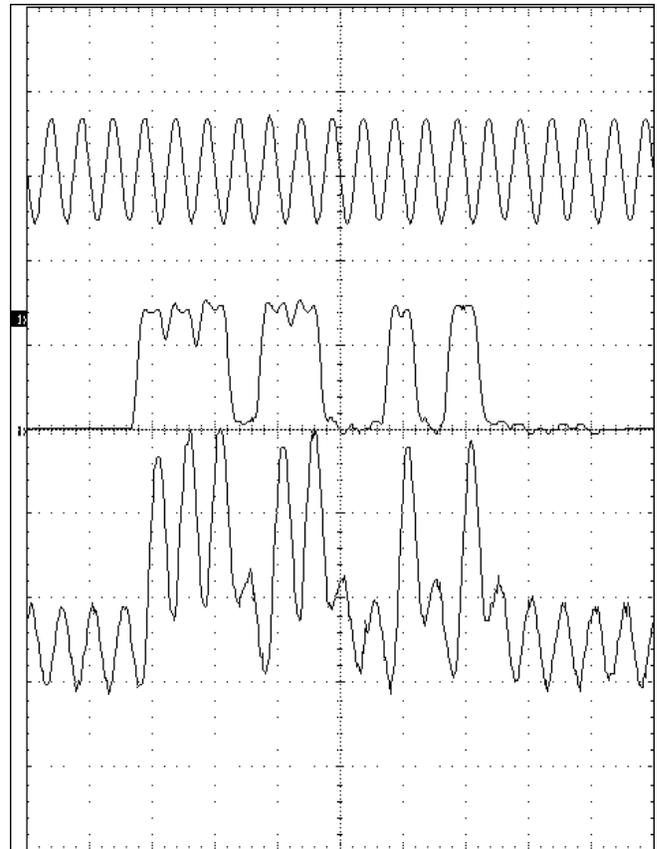


Fig. 5. Waveforms captured during the operation of a single shift register at 2 GHz using an NRZ input signal produced by combining two 1-GHz RZ channels from a word generator. The horizontal scale is 1 ns per division.

experiments are described in detail later in this section. Although we were able to show that the filter can perform the correlation function, two problem areas were identified: (1) very low signal amplitudes in the summing bus and (2) a high level of direct feedthrough between sections of the circuit. These two issues are also discussed below.

### A. High Parasitic Inductances

Parasitic inductances were found to be significantly larger than had been expected, greatly reducing the signal coupling efficiency of the NDRO tap-weight circuit. A test version of the tap, configured as a SQUID, was used to measure the mutual inductances with great accuracy and to estimate the self inductance and  $Ll_c$  product of the loop. Fig. 6 shows a close-up of the tap layout. It consists of an inductive loop in layer M4, the metal layer with the lower specific inductance because it is closest to the ground plane. Two transformers couple to this loop with windings in M2 metal. The winding at the top comes from the sampler and carries the current representing the stored signal sample. The winding at the bottom is part of the summing loop, which accumulates the magnetic flux from all of the taps and generates the current sensed by the QFP. In the test SQUID, external currents

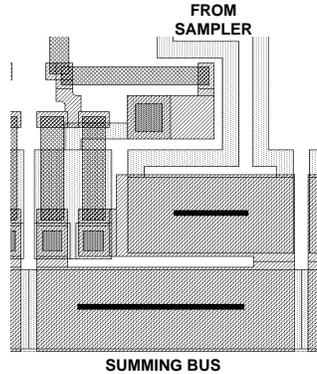


Fig. 6. Detailed view of the NDRO tap circuit, in which the black bars superimposed on the layout indicate the effective lengths of the input and output transformers that contribute to the mutual inductance.

could be applied to both of these windings. Note that each slice contains two tap circuits, one for each of the samplers that comprise the T/H cell.

By comparing and analyzing the mutual inductance values for the two transformers, we could determine the effective lengths of the M2 windings, and they are indicated by the narrow black rectangles superimposed on Fig. 6. The values are substantially less than the physical lengths. It appears that for lines of width  $W$ , a length of approximately  $W/2$  at each end does not couple effectively, probably because the current flow is no longer parallel to the length of the conductor.

The inferred value of mutual inductance per unit length came out close to the value computed by our inductance simulation software. The calculated self inductance corresponding to that mutual inductance is substantially less than the total self inductance estimated by fitting the SQUID threshold curves, suggesting that corners, vias, and contacts to junctions contribute a significant parasitic inductance.

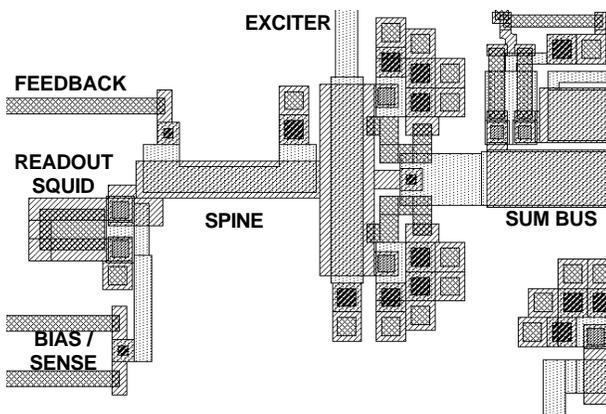


Fig. 7. Detailed view of the readout QFP. The current induced on the summing bus is injected directly into the spine of the QFP. At the same time feedback current couples flux inductively into the spine. Note that this version of the filter is slightly different from the one shown in Fig. 4, where the summing bus current is inductively coupled rather than directly injected.

## B. Measurement Technique

Because of the reduced coupling in the tap circuits, the output signal levels in the summing bus, which were expected to be low even in the ideal case, were even lower. Two experimental techniques were employed to measure these very low-level filter outputs with great precision.

First, a special technique for using the QFP was developed to make extremely sensitive measurements of current in the summing bus. A detailed view of the layout of the QFP sense circuit is shown in Fig. 7. The QFP has two inputs: a directly injected current at the top of the spine inductor and an inductively coupled current along the spine. Because the QFP is approximately three times more sensitive to directly injected current than to inductively coupled current, the summing bus of the filter is connected directly to the QFP in the version used for the experiments reported here (an older version is shown in Fig. 4).

A measurement is made by applying a pulse to the exciter input to the QFP. This causes the QFP to latch into one of two stable states with nearly equal-amplitude but opposite-direction currents in the spine. The asymmetric readout SQUID is then activated to sense the sign of that current by switching into the voltage state in one case and remaining in the superconducting state in the other. A feedback current applied to the inductive input to the QFP is adjusted to keep the QFP right at its threshold point, where it switches exactly 50% of the time into each of its two states. A digital circuit with an up-down counter and a digital-to-analog converter (DAC) to generate the feedback current could be used to automate the measurement, but we did it by eye as follows. The output pulses from the readout SQUID were displayed on an oscilloscope with the time axis expanded to show an interval during which only the two stable readout levels—and none of the switching transients—occurred. The feedback current was then adjusted to make the two traces appears to have exactly equal brightness. This procedure was found to give repeatable results with a sensitivity of about  $0.2 \mu\text{A}$ , equivalent to about  $0.07 \mu\text{A}$  of current in the summing bus.

The second technique to improve the sensitivity with which the filter response could be measured was to vary the input signal amplitude over its full dynamic range and record the feedback current. A straight-line fit between the output and input gives an even more sensitive measure of the responsivity of the filter.

## C. Signal Feedthrough

Besides the problem of low signal levels in the summing bus, we also observed direct feedthrough to the output from every other pin on the chip. The output was measured as dc signals were applied to each of the input signal and clock lines. Feedthrough from the analog signal line was typically about  $0.013 \mu\text{A}$  of QFP feedback current per  $1 \mu\text{A}$  of input

signal current (1.3%). Some of this feedthrough could be the result of mismatch between the two samplers in the T/H. Feedthrough from the T/H reset line was about 0.7% and from the T/H buffer clock about 0.3%.

We had observed feedthrough of this type earlier—even from currents applied to completely independent circuits on a chip—and thought we understood its origin in ground-return current spreading among all the ground pins on the chip. However, the behavior seen here was not in accord with our theory. The filter test circuit was on a piece of ground plane that spanned the chip, a situation that would be expected to give rise to feedthrough. When we cut one end of that ground strap, however, the feedthrough did not disappear; in fact, it changed little. Thus, the exact source of the feedthrough remains a mystery. We now suspect that it may result from magnetic fields generated by wires in the cryoprobe running perpendicular to the chip and thus generating magnetic fields parallel to the surface of the chip.

#### D. Functional Verification and Calibration

Since the operation of the complete filter is a complex process, we approached it step by step, verifying sequentially that each piece of the chip was working. To avoid the problem of the feedthrough discussed in the previous section, wherever possible we used waveforms that could be pulsed and then removed while the output was detected. For example, the first check was that the buffers between the sampling control shift register and the T/H cells were operating properly and had enough output to drive the active sampler. In this case we raised the input analog signal to the desired value, then pulsed the clock line to the buffer to force it to switch momentarily to the voltage state. This should

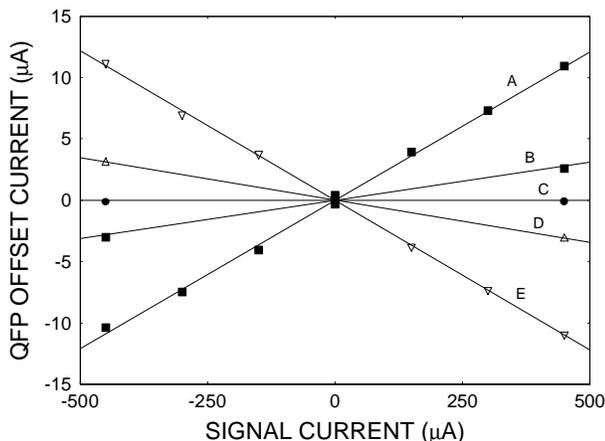


Fig. 8. This plot illustrates the response of the filter when all samplers and all taps were operated in parallel. Curve A shows the response when the T/H buffer was clocked to take normal samples; curve E shows the response when the RESET line was clocked to invert the roles of the two samplers in the T/H cells. Curve C shows the response when both the buffer clock and RESET were pulsed, causing the samples in the two samplers to cancel each other. Curves B and D correspond to the conditions with curves A and E, respectively, when all tap weights were set to ‘0’ by dc biasing the tap buffer clock line.

latch the signal level into all seven T/H cells. The analog signal was then removed, eliminating all sources of feedthrough. At that point the QFP was exercised as described in section B. Measurements were taken over a wide, bipolar range of input signals; the result was curve A in Fig. 8.

As can be seen in Fig. 4, each T/H cell contains two samplers, one of them serving as a reference channel to cancel out common-mode signal [4]. The line marked RESET in Fig. 4 can be used to reverse the roles of the two samplers. This was done by pulsing the RESET line instead of the T/H BUF CLK line. The response of the filter, which should be the same but with the opposite sign, is shown in curve E in Fig. 8. Finally, curve C is obtained when both RESET and the T/H buffer clock are pulsed; the signals in the two samplers should cancel.

The next step was to test the operation of the taps. By applying a sufficiently high current to the clock line that biases the buffers on the outputs from the reference code shift register, all the taps can be made to switch to the ‘0’ state. This can be done for the signal sampling modes corresponding to both curves A and E, giving the results shown in curves B and D, respectively. Clearly, the tap weight in the nominal ‘0’ state is not zero. It should be noted that there is a feedthrough signal associated with the dc bias on the tap buffers (which must remain biased for a weight of ‘0’), and this has been taken out in Fig. 8 by shifting each curve vertically to make it go through the origin.

So far none of the experiments depended on the operation of the shift registers. The final characterization experiments before we attempted to run the entire filter checked the operation of the shift registers. Output lines from the registers verified that data was passing through them; the only remaining question was whether the shift register outputs would trigger the buffers (in the previously described experiments the buffer clock was driven to a high enough level that the buffer fired without any input from the shift registers). In one experiment a pattern with a single 1 was loaded into the sampling control register and then the buffer clock was pulsed to store a signal level into the selected T/H cell. The slope of the output as the signal amplitude was

TABLE I. Responsivity of each slice (channel) of the prototype filter. All slices were operational, and the responsivity was quite uniform, with a possible slight difference between the four slices on one side of the filter (the first four entries in the table) and the three slices on the other. The error values are from the least-square-error fit to the response data.

SIGNAL PATTERN	RESPONSIVITY
1000000	0.0032 ± 0.0005
0100000	0.0032 ± 0.0001
0010000	0.0033 ± 0.0002
0001000	0.0033 ± 0.0002
0000100	0.0037 ± 0.0006
0000010	0.0035 ± 0.0005
0000001	0.0038 ± 0.0001

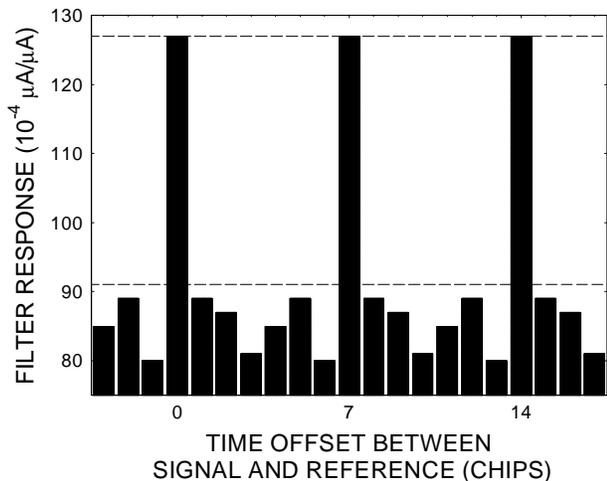


Fig. 9. Correlation response. The two dashed lines are the peak and sidelobe levels expected.

varied is shown in TABLE I. This experiment established that the analog registers in all seven slices were working and had nearly equal gain. One thing the table does not show is the dc offsets. They varied over a peak-to-peak range of about 1  $\mu\text{A}$ , corresponding to about 50% of the peak-to-peak response to the signal. Clearly, this level of feedthrough is not acceptable and will have to be reduced.

A similar experiment was performed with the reference code register to verify that each tap could be addressed.

#### E. Correlation of a Seven-Chip PN Code

For the final experiment the pn code sequence “1110100” was used. A unipolar input signal with amplitude A for the 1s and zero for the 0s was applied while a single 1 was propagated through the sampling control register. This loaded the signal pattern into the array of T/H cells. Concurrently, the time-reversed pattern “0010111” and its time-shifted versions (“1001011”, “1100101”, etc.) were loaded into the reference code register. For each reference pattern the filter output was then measured as described earlier over a range of analog signal amplitudes. The responsivity of the filter (change in output per unit change of input) is plotted in Fig. 9 as a function of the number of chips by which the reference code was rotated from alignment with the input signal. For the sample used in this experiment, the signal leakage through a tap with a nominal weight of zero was measured to be about 43.5%.

Table II shows the theoretical peak response (offset modulo 7 = 0) and sidelobe response (offset modulo 7  $\neq$  0) for unipolar and bipolar input signal patterns and unipolar tap weights with and without the observed level of leakage. We could have achieved a two-times larger response from the test filter by using a bipolar signal, but it would have been harder to generate a well-balanced, variable-amplitude

TABLE II. Peak and sidelobe response levels for the 7-chip pn code “1110100” for combinations of two types of input signals—unipolar (values of +1 and 0) and bipolar (values of +1 and -1)—and for unipolar taps with perfect weights of 1 and 0 and leaky weights of 1.000 and 0.435.

TAP QUALITY	SIGNAL TYPE			
	BIPOLAR		UNIPOLAR	
	PEAK	SL	PEAK	SL
PERFECT	4.00	0.00	4.00	2.00
LEAKY	2.70	0.44	4.00	2.87

bipolar signal. Our measurement technique was sensitive enough to work with a unipolar signal.

The response with all channels active was used to obtain a per-channel responsivity, which was then multiplied by 4.00 and 2.87 to give the levels shown as horizontal dashed lines in Fig. 9. The sidelobes all fall below the expected level probably because our estimate of the tap leakage was too high. A value of 34% instead of 44% would give a sidelobe level of 85 instead of 91.

## VI. SUMMARY

In the past we had demonstrated the functionality of each individual element of a superconductive programmable binary-analog matched filter for a 2-Gchip/s direct-sequence spread-spectrum modem. Now all of these elements have been operated together in a complete prototype filter in low-frequency tests. The filter produced the correct output for a 7-chip pseudo-noise (pn) code sequence. Two significant problem areas were identified: low signal levels aggravated by larger-than-expected parasitic inductance effects and direct feedthrough of clock and control currents to the filter output.

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