Mixed Analog-Digital Niobium Superconductive Circuits for a 2-Gigachip-per-Second Spread-Spectrum Modem

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Abstract—This paper describes the architecture and operation of a superconductive programmable matched filter that provides rapid synchronization information and data demodulation for a 2-GHz spread-spectrum modem. Results are reported for the first circuit fabrication runs using a new doubly planarized process. With the exception of circuits containing layout errors, all circuits have performed as intended and with characteristics that match well the predictions of JSIM simulations. The MVTL digital components and the buffer between the digital and analog circuits have been demonstrated for the first time. The seven-stage MVTL shift register in a complete prototype filter was operated at 1 GHz. In addition, combinations of (1) the MVTL digital shift register and the buffer and (2) the buffer and the T/H cell have been operated successfully, demonstrating that all of the components in the filter core will work together.

I. Introduction

At earlier Applied Superconductivity Conferences [1,2] and at a Government Microcircuit Applications Conference [3] we presented the architecture of a 2-gigachip-per-second direct-sequence spread-spectrum modem and described the operation of the core analog subcircuits in the analog-binary programmable matched filter for such a modem. Those modules included analog sampler and track/hold (T/H) circuits and a nondestructive-readout (NDRO) binary-weighted analog tap circuit. In this paper we present the first modem circuit test results for chips fabricated in our "doubly planarized all-refractory technology for superconductors" (DPARTS) process. Two runs have produced devices with high yield, good quality, and on-target parameter values. Circuits have been exercised both at low frequencies and at frequencies up to 1 GHz, and they have performed as intended and in agreement with simulations using the JSIM circuit simulator.

II. Programmable Filter Architecture and Operation

The modem's receiver channel requires a programmable matched filter (correlator) for establishing time synchronization between the receiver and the transmitter and for demodulating (despreading) the transmitted signal. A high-level block diagram of the filter is shown in Fig. 1.

The upper section of the filter contains a bank of analog T/H cells (the analog data register) and a digital shift register (the sampling control register). The shift register is loaded with all 0's except for a single 1, which serves as an index. Where the 1 appears, the corresponding T/H cell takes a new sample. This 1 circulates through the shift register, causing successive analog samples to be taken in successive T/H cells. Thus, at any given time the most recent N samples of the input signal are stored in the analog data register, with the newest sample at the index, progressively older samples to the left and wrapping around to the right, and the oldest sample just to the right of the index. Note that the signal samples do not move through the register. Rather, each one remains in place for N clock cycles, at which point it is replaced by a newer sample.

The lower section of the filter contains a bank of tap weight cells and a shift register (the binary reference register), which is loaded with a time-reversed copy of the code that was used in the transmitter to spread the signal. Each tap multiplies the analog sample stored in the corresponding T/H cell by either +1 or -1 (or, alternatively, +1 or 0) depending on the bit stored in the reference register. As the two shift registers are clocked synchronously, the reference code moves past the stationary samples of the input signal. When the reference code aligns with the received signal, a correlation peak occurs. The output peaks strongly in a positive direction for an encoded signal bit of 1 and in a negative direction for a signal bit of 0. The position in time of the correlation peaks provides synchronization information, while the polarity of the output peaks provides the demodulated data. Note that in the course of operation, the signal stored in a T/H cell, which changes only every N clock cycles, is multiplied by a sequence of varying reference bits. Consequently, the tap-weighting process must be nonde-

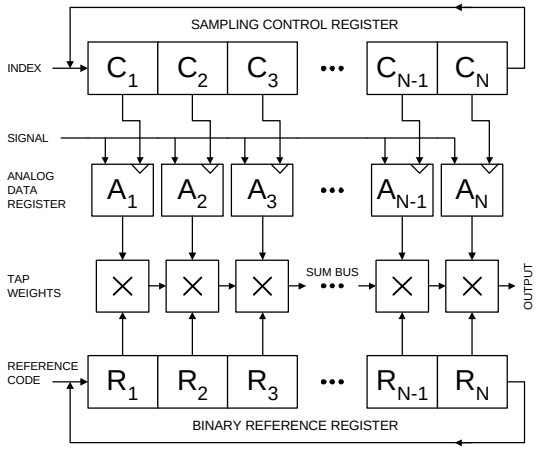

Fig. 1. Block diagram of the superconductive programmable matched filter.

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structive; that is, it must not alter the stored analog samples.

For each bit (or "chip" in spread-spectrum terminology) of the spreading code, the filter contains an identical section called a slice. Figure 2 shows a block diagram of the first slice along with the output summing and detection circuit. This diagram includes some additional details of the implementation and follows more closely the actual layout of the circuit. First, it indicates that the digital shift registers are implemented using modified variable threshold logic (MVTL) gates [4]. Second, because driving the analog components—the samplers and the taps—requires significant currents at voltages well above the gap voltage, some form of buffer circuit is required between the shift register outputs and the inputs to the analog cells. Third, the figure indicates that the output summing bus is implemented by connecting all the taps to a common inductor loop, whose flux is detected by a quantum flux parametron (QFP) circuit.

Finally, the figure shows that the T/H circuit is implemented as a pair of samplers, whose outputs are balanced. Each sampler alone, as described in [1], stores its sample in the form of an offset from a replica of the applied signal. Thus, alone it produces a valid output only when the input signal is subsequently removed (forced to zero), a requirement that cannot be met in the modem filter, which must process data continuously. The feedthrough of the input signal is canceled by the reference sampler, which is activated momentarily via the RESET line when the chip is first cooled and before an input signal is applied.

III. Circuit Design

Figure 3 shows a circuit schematic for the T/H portion of the filter slice. The digital shift register follows the design of Meier and Przybysz [5] except that the AND gates were omitted. It is intended to operate using three-phase, offset-sine-wave clocks. With such clocks, the total current into ground is constant to first order, thereby minimizing high-frequency voltage fluctuations in the ground-plane metal (ground bounce).

The voltage-amplifying buffer uses stacks of two junctions to reach an output level approaching twice the gap voltage, as required to switch the sampler and tap circuits. For our test designs, a separate clock was provided for the buffer, though it can ultimately share one of the shift-register clocks.

The two samplers in the T/H cell are as identical as one can make them to minimize the common-mode feedthrough of the input signal, which is applied to both samplers but in opposite directions. Although the inductors in the input and output arms of each sampler are drawn using the same symbol in the schematic, the inductors on the input side are in fact much larger than those on the output side. The secondary inductors of the output transformers are the loop inductors of the tap-weight cells, and those inductances, as discussed next, must be extremely small. The two sampler outputs are combined in the tap cell.

The schematic of the tap-weight section of the slice is not shown here but is very similar to Fig. 3. In our initial layout, it uses the same MVTL shift register and buffer designs. The tap circuit is the same as the sampler circuit except for parameter values. While the sampler cell has a loop inductance large enough to store several tens of flux quanta ($_0$ = 2.07 mA-pH), the tap circuit's loop inductance and

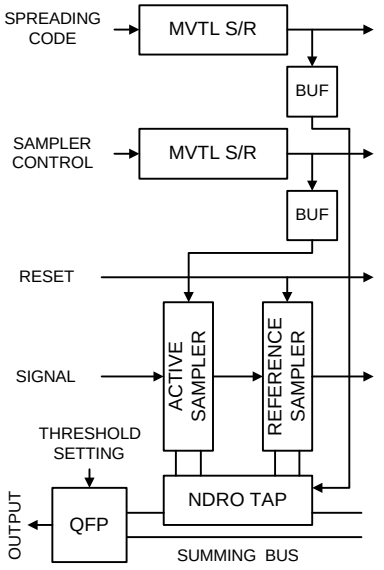

Fig. 2. Detailed block diagram of one slice of the filter along with the output detector circuitry.

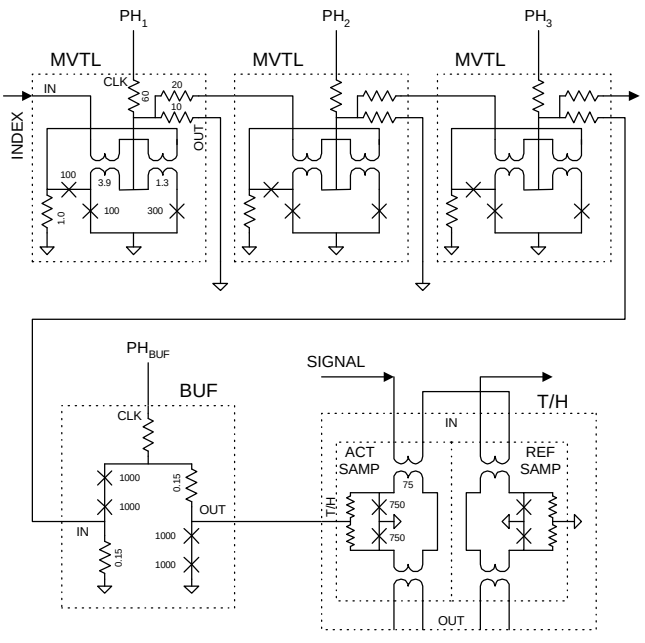

Fig. 3. Circuit schematic of the T/H channel of the filter, including the MVTL shift register, the buffer, and the T/H circuit. The component values shown are nominal values, and damping resistors across the junctions are not shown. Resistances are in ohms, junction critical currents in microamperes, and inductances in picohenries.

junction critical currents are so low that not even one fluxon can be stored ($L \cdot I_c \approx 0.25\ \Phi_0$). As with the T/H cell, the tap-weight cell has two subcircuits. One is connected to each of the samplers, but both are driven by the buffer output. When the buffer has not switched to the voltage state, the two signals from the samplers pass through the tap and add in the summing bus, giving a weight of +1. When the buffer has switched, its output drives the junctions in the tap circuit into the resistive state, quenching any circulating currents and giving a tap weight of 0.

IV. Circuit Tests

The mask set for the first modem test circuit run using the DPARTS process was designed to complete the demonstration of the basic circuit components and to address the interfaces between them. Although we did not expect the first design of complete circuits to operate successfully, we nevertheless included both a full filter slice and a complete seven-chip filter. Their main purpose was to ensure that the layouts of the components were consistent with the very tight packing required in the filter. In fact, the limited number of pins available on the chips in the mask set prevented us from connecting all of the signal lines from those circuits to external pins.

A. MVTL Circuits

Although MVTL shift registers have been operated elsewhere, this was our first MVTL implementation. To allow us to characterize the design fully, we included the following range of test circuits:

- SQUID from OR gate
- OR gate
- one-stage (three-gate) shift register (with buffer)
- seven-stage shift register (in full filter)

The MVTL SQUID comprised an MVTL OR-gate from which the data-injection junction connecting the input line to the SQUID loop was omitted, leaving a pure asymmetric SQUID. It was measured on our automatic SQUID threshold tracer, and the results were compared to calculated curves in order to determine the parameter values for the circuit. Figure 4 shows the measured SQUID characteristic along with what we judged to be the best theoretical fit.

The total mutual inductance value, 2.77 pH, can be determined with great accuracy from the period along the control-current axis. Similarly, the total critical current, 325 μA, is a sensitive parameter in the theoretical fit. Since noise suppression of the critical currents might give apparent values lower than the true values, we looked for theoretical fits that matched the outer boundaries of the measured data distributions.

Determining the total loop inductance and the ratios of inductance and critical current in the two arms of the SQUID is more difficult because the theoretical results do not change dramatically as those parameters are varied. The I_c ratio was designed to be 3. Since the layout used four identical small junctions, with three in parallel on one side, the design ratio was highly likely to have been achieved. This was confirmed by the fact that significant variations in the ratio in either direction from 3 degraded the fit.

Getting the inductance values was especially difficult. The theoretical curves in Fig. 4 were calculated for a total loop inductance of 4.4 pH distributed between the arms in the ratio 1.5 to 1. However, good fits were also obtained with L=4.2 pH and a ratio of 1.4 and with L=4.6 pH and a ratio of 1.6. We attempted to estimate inductance values from theoretical calculations using the INDUCTAN computer program, but because inductances are not well known for corners in the layout, the estimates were crude. We arrived at L=4.3 pH with a ratio of 1.55, reasonably consistent with the values from fitting the SQUID characteristic.

The inductance ratio is considerably less than the target value of 3, but, as will be seen, this did not have a significant effect on the performance of the circuits. The value was low because the paths from the junctions to ground contributed substantial additional inductance equally in each arm. This is also why the ratio of M to L (2.77/4.4=0.63) is significantly less than the calculated M/L ratio of approximately 0.9 for the transformer parts of the circuit.

The next tests were performed on an isolated MVTL OR gate (*i.e.*, one with no load on the output). The minimum clock current amplitude required to switch the gate was measured as a function of the input signal current. Figure 5 shows the results. We then used the JSIM circuit simulator to calculate the expected margins. The circuit parameters determined from the SQUID measurement were used except for the total critical current, which was adjusted to make the clock margin at zero signal agree with the experimental result. The fit, as can be seen in Fig. 5, is excellent.

We did learn that JSIM results are not always reliable. For

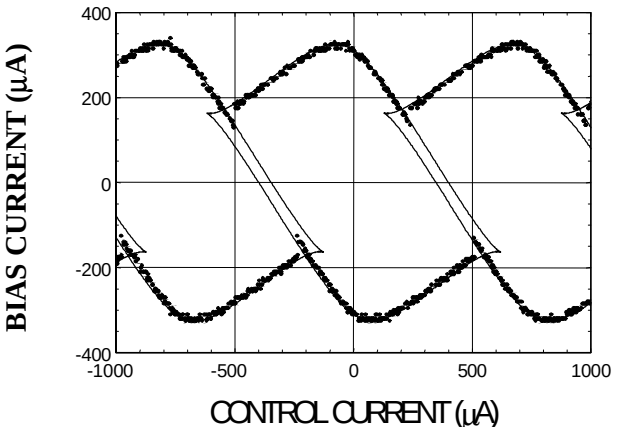

Fig. 4. Experimental MVTL SQUID characteristic (points) with overlay of best theoretical fit (solid curves). The bias current corresponds to the clock current of the MVTL gate, while the control current corresponds to the input signal current.

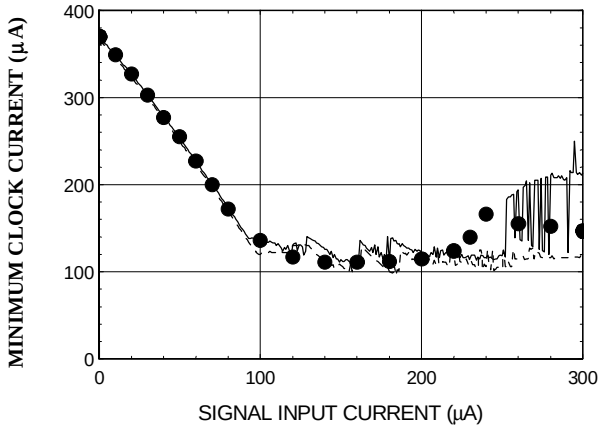

Fig. 5. Clock margin for an isolated MVTL OR gate. The points are measured values. The solid curve was calculated using the JSIM simulator with a simulation interval of 10 ns, while the dashed curve was for a simulation interval of 50 ns.

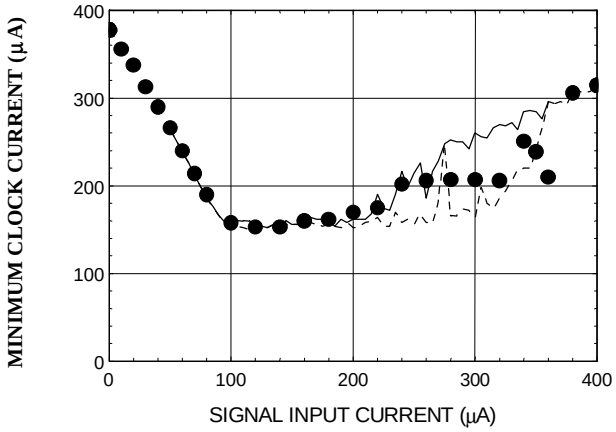

Fig. 6. Clock margins for a loaded OR gate in a shift register. The points are measured values. The dashed, lower curve is the lowest clock voltage at which a JSIM simulation showed the gate switching, while the solid, upper curve shows the lowest clock voltage for which a JSIM simulation showed the gate not switching. Between the two curves simulations sometimes showed the gate switching and sometimes not.

input currents above the critical current of the data-injection junction (92 μA in these simulations) JSIM becomes unstable (chaotic); the results change drastically for small changes in the simulation parameters. These instabilities are particularly evident in Fig. 5 for the simulations over a 10-ns time period with input currents above 250 μA. This is an unusual situation in that one is looking for the point at which the SQUID junctions switch when another junction in the circuit has already switched and is generating very high frequency Josephson oscillations.

The next MVTL circuit tested was a fragment comprising the circuit shown in Fig. 3 but without the T/H cell. This test circuit had lines for monitoring the outputs of each OR gate individually and a line for driving the buffer directly from a pin on the chip. The clock margin of a loaded OR gate was measured by clocking only the first gate while monitoring its output. The results are shown in Fig. 6. Although the loading was the equivalent of a fanout of 3, the margins are still very large, ±42% for inputs near 130 μA. Figure 6, like Fig. 5, shows the results of JSIM simulations, and again the results agree very well.

The final MVTL shift register test was performed with the complete seven-stage filter prototype. It was operated first at low frequency with pulse clocks and then at frequencies of 400 MHz and 1 GHz with sine-wave clocks. As noted earlier, not all signal lines in the filter were brought out to pins on the chip. In particular, partly owing to an oversight, there was no connection to the input of the shift register, and a trick had to be used to demonstrate its operation. At intervals well in excess of seven clock cycles, the amplitude of a single positive cycle of one clock phase was raised to a level above the MVTL upper clock threshold. This caused the corresponding gates in all stages of the shift register to switch to the 1 state. The subsequent output from the shift register should, thus, be seven 1's followed by 0's.

The complex clock patterns required for the high-speed versions of this experiment were produced as follows. A frequency synthesizer generated a master sine wave, which was split into three parts. Adjustable delay lines were set to make the phases fall at 120° intervals, and attenuators were used to adjust the amplitudes to the proper level for shift register operation. Bias tees provided dc offsets. A subharmonic output from the synthesizer was used to trigger a very fast pulse generator, whose output was combined with the sine wave for the phase-1 clock. The timing was adjusted with a variable delay line to place the pulse right on the peak of a sine-wave cycle.

Figure 7 shows the 1-GHz clock waveforms recorded on a Tektronix TDS 684B digital oscilloscope. Despite the scope's rated bandwidth of 1 GHz, the traces were significantly attenuated. Since the true signal levels could not be observed accurately at 1 GHz, the experiment was first performed at 400 MHz. Then the frequency of the synthesizer was raised, and the delay lines were readjusted to establish the correct phasing. The shift register continued to work with almost no modification to the clock amplitudes and

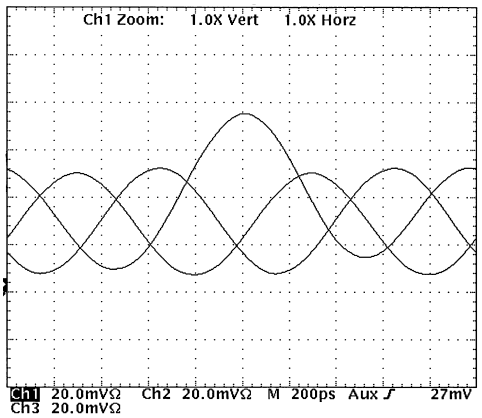

Fig. 7. Traces from a digital real-time oscilloscope showing the three-phase sine-wave clocks with the extra offset added during one cycle.

offsets.

Figure 8 shows the outputs from the shift register at clock frequencies of 400 MHz and 1 GHz as observed on a Tektronix 9104 oscilloscope. Because of the 1-GHz bandwidth, the outputs are rounded and attenuated. However, the expected series of seven pulses is unmistakable. Because of the tricky adjustments required to generate the clock waveforms, we have not yet attempted the experiment at frequencies above 1 GHz.

B. Buffer Circuit and Sampler

Three important circuit tests were performed using the buffer. Two of them used the circuit described earlier with one three-gate stage of the shift register driving a buffer. A separate connection to the line coupling the last MVTL OR gate to the buffer could be used to drive the buffer directly. The margins on the buffer clock could then be measured as a function of input signal to the buffer. The results are shown in Fig. 9. We also operated the shift register and allowed it to control the buffer. It did so successfully, but the margin on the buffer clock was very narrow (~80 μA). This was partly the result of a layout mistake. Each OR gate has two output resistors, one of 10 and one of 20 . The larger resistor was supposed to drive the next stage of the shift register with about 100 μA, while the smaller one would drive the buffer with about 200 μA. In the layout the connections were reversed. However, even 200 μA of drive would provide an uncomfortably small margin, and the addition of an MVTL AND gate will probably be tried in a future design.

The most critical issue with the buffer was whether its output would be strong enough to drive the sampler into track mode. For this purpose, the test chips contained a circuit fragment comprising the buffer and T/H cell from the schematic in Fig. 3 with a dc SQUID on the T/H output to sense the current stored in the T/H cell. With a dc input applied to the buffer, the buffer clock line was pulsed to put

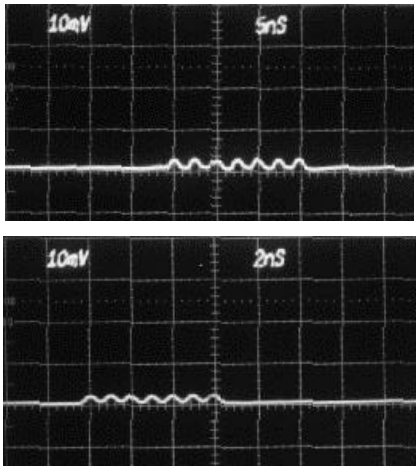

Fig. 8. These oscilloscope photos show the output from the MVTL shift register in the complete seven-stage filter. The clock frequencies were 400 MHz for the top photo and 1 GHz for the bottom photo.

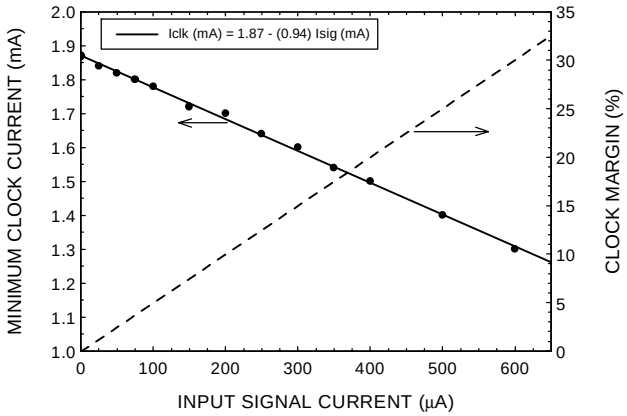

Fig. 9. Clock margins for the buffer between the digital shift registers and the analog components. The points are measured data. The solid curve is a least-squares fit to a straight line, with the equation shown in the legend.

the T/H cell momentarily into track mode to acquire a new sample. As the input signal to the T/H was varied, one could see the output snapping to the new value with each pulse to the buffer.

The photo in Fig. 10 shows the output waveforms from the dc SQUID while hundreds of samples were taken. The vertical displacement of the trace corresponds to the stored current in the T/H loop, and one can clearly see the expected quantization. The quantum of loop current is $_0$/L, where $_0$ is the flux quantum (2.07 mA-pH) and L is the loop inductance of each sampler.

Since the photo in Fig. 10 was taken with a dc input signal, it illustrates a potential problem with the sampler: quantum jitter. It suggests that when the track signal from the buffer to the sampler returns to zero, the current in the sampler loop does not always settle in the quantum state closest to zero current (the quantum levels are displaced by flux from the external signal current). One would expect one or two values, depending on whether the zero current level during track mode falls close to a quantum level or near the midpoint between two levels. In earlier experiments with samplers driven by external signals [1,3] there appeared to be less quantum jitter. A new damping arrangement was

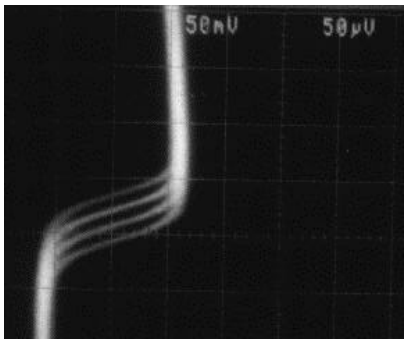

Fig. 10. Oscilloscope photograph showing a superposition of numerous outputs from the dc SQUID monitoring the samples stored in the T/H cell. The quantization of the stored samples can be seen clearly.

tried in these test circuits, and perhaps it did not provide adequate damping of the junctions.

Because the dc SQUID included a second control line nearly identical to the line from the T/H cell, it was possible to obtain an absolute calibration of the output in terms of the current in the sampler loop. Figure 11 shows sets of output values for several input signal levels. The curve fit gives a quantum step of 14.67 μA in the control line current. Since the control line couples as strongly as both samplers in the T/H, this corresponds to a current step of 29.34 μA in the active sampler and a loop inductance of 70.5 pH. The value estimated from INDUCTAN calculations was about 75 pH, in good agreement.

V. Conclusions

The first DPARTS wafer fabrication runs containing test circuits for the programmable filter for a 2-GHz spread-spectrum modem have been completed successfully. With the exception of circuits containing layout errors, all circuits have performed as intended and with characteristics that match well the predictions of JSIM simulations. The MVTL digital components and the buffer between the digital and analog circuits have been demonstrated for the first time. The seven-stage MVTL shift register in a complete prototype filter was operated at 1 GHz. In addition, combinations of (1) the MVTL digital shift register and the buffer and (2) the buffer and the T/H cell have been operated successfully, demonstrating that all of the components in the filter slice will work together.

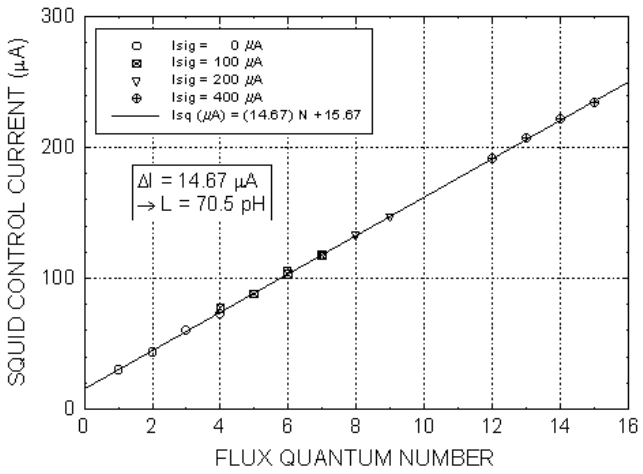

Fig. 11. Plot showing the current in the control line of the dc SQUID output detector corresponding to a range of quantum states in the T/H cell. The total inductance in the sampler storage loop can be determined accurately from the size of the quantum step in current.

References

[1] J. P. Sage, J. B. Green, and A. Davidson, "Design, fabrication, and testing of a high-speed analog sampler," *IEEE Trans. Appl. Supercond.*, vol. 3, no. 1, pp. 2562–2565, March 1993.

[2] J. P. Sage and R. W. Ralston, "Niobium superconducting circuits for a 2-gigachip-per-second spread-spectrum modem," paper ESD-11 at the 1994 Applied Superconductivity Conference (unpublished).

[3] J. P. Sage and R. W. Ralston, "Superconducting circuits for a 2-gigachip-per-second spread-spectrum modem," Government Microcircuit Applications Conference, 1993 Digest of Papers, pp. 565–568, November 1993.

[4] S. Kotani, N. Fujimaki, T. Imamura, and S. Hasuo, "Ultrahigh-speed logic gate family with Nb/Al-AlO_x/Nb Josephson junctions," *IEEE Trans. Electron Devices*, vol. 33, pp. 379–384, March 1986.

[5] D. L. Meier and J. X. Przybysz, "Performance of MVTL OR-AND gates when data precedes bias," *IEEE Trans. Appl. Supercond.*, vol. 3, no. 1, pp. 2736–2739, March 1993.