Demonstration of Charge-Coupled Devices in Fully Depleted SOI

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Abstract

We have demonstrated what we believe to be the first charge-coupled devices implemented in an SOI process.

Introduction

Charge-coupled devices (CCDs) are an important analog signal-processing circuit element [1]. They are, in essence, field-effect transistors with a large number of adjacent gates between the source and drain. Properly timed clock voltages applied to those gates cause discrete packets of charge in the CCD channel to move from gate to gate.

We have used bulk silicon CCDs to achieve very low power analog-to-digital converters [2]. In one application they are part of an integrated imager, performing direct conversion of pixel charges from a CCD image sensor to digital data [3][4]. By combining the charge-to-digital converter with a wideband charge-domain voltage-to-charge sampler, we have implemented general-purpose A-to-D converters [5].

A fully depleted SOI (FDSOI) implementation would offer advantages in two areas. Low parasitic capacitance along with the strong drive of FDSOI transistors would improve the speed and power performance of clock drivers and auxiliary analog circuits, such as sense amplifiers and comparators. Digital modules for timing and clock generation, autonomous calibration, and post-processing of data to improve linearity would also operate faster and with lower power consumption.

In addition, CCDs implemented in FDSOI are expected to operate up to higher speeds than conventional bulk surface-channel CCDs. While FDSOI CCDs retain the high linearity and charge storage density of surface-channel CCDs, the buried oxide (BOX) layer allows strong fringing electric fields to penetrate beneath the gates and accelerate the transfer of charge from gate to gate. The simulation results in Fig. 1 illustrate the speed improvement with increasing BOX thickness. The improvement saturates when the BOX thickness becomes comparable to the gate length.

CCD Gate Fabrication Process

Complete transfer of charge from one gate to the next depends on a monotonic gradient in the channel potential between the gates. This requires that the gaps between gates be sufficiently small. Nearly all CCDs made in the past have used two or more overlapping layers of polysilicon. As device dimensions, including gate oxide thicknesses, have shrunk, this approach has become less and less feasible. Close matching of gate characteristics requires that all gates be fabricated from a single layer of polysilicon over a single gate insulator.

We have developed a new process for fabricating gaps within the gate layer that are much smaller than the smallest lithgraphic feature supported. The sequence of steps is illustrated by a set of scanning electron microscope (SEM) photographs in Fig. 2. It begins with a continuous 200-nm-thick layer of polysilicon on top of a 4.2-nm gate oxide in the areas that will become CCDs.

Definition of the gaps starts when a 200-nm layer of TEOS (tetra-ethyl-ortho-silicate) oxide is deposited and patterned with openings that are nominally 200 nm wider than the intended final gap width. Figure 2A, shows a pattern of oxide strips about 160 nm wide with gaps of about 240 nm between them (corresponding to a gate pitch of 400 nm).

Next, an additional 100 nm of TEOS oxide is deposited and etched—without using a mask—to form a nominally 100-nm-wide spacer around the original TEOS pattern. This reduces the width of

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the original openings by 200 nm (nominally). The SEM photograph in Fig. 2B shows an opening that is about 260 nm wide at the top but only 90 nm wide at the bottom. This oxide layer serves as a hard mask for a highly anisotropic etch of the polysilicon. Figure 2C shows the resulting polisilcon layer with gaps that are about 90 nm wide.

A very important feature of this process, particularly for development purposes, is that the gap width is controlled directly by features drawn on the mask, and gaps of many different dimensions can be fabricated within the same mask set. Figure 2D, for example, shows gates in another part of the wafer with a gap of only 23 nm.

The most challenging step in the process is removal of the thick oxide hard mask without attacking the very thin gate oxide exposed in the gaps. This is done by protecting the gaps with photoresist while etching the hard-mask oxide, as shown in Fig. 2E. When the resist is then removed, the CCD gate structure is complete, with very narrow gaps in a single layer of polysilicon (Fig. 2F).

CCD Circuit Designs

Because CCDs had not previously been demonstrated in FDSOI and because the process for forming narrow gaps was new, we designed the initial test chip to explore a wide range of design parameters: nominal gap widths from 0 to 200 nm in 10-nm steps, CCD shift registers from 1 to 200 stages long, and gate length pitches from 400 nm to 1500 nm.

All of the CCDs were based on a very simple design that required the smallest number of applied signals. They used three clock phases, which also operated the voltage-to-charge sampler at the input and the charge-to-voltage readout circuit at the output. Figure 3 illustrates the topology of the CCDs and the channel potentials at one step in the clock sequence. Measurements at modest frequencies (clock rates up to 150 MHz) have shown very good performance. The sequence of output pulses from the longest shift register are shown in Fig. 4. While improvements are still needed, the devices show very promising performance. FDSOI CCDs are expected to operate at clock rates in the gigahertz range.

References

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[4] M. P. Anthony et al., "Charge-Domain Analog-to-Digital Converter for a Charge-Coupled Device Imager Focal Plane," Solid State Research Report, Lincoln Laboratory, Massachusetts Institute of Technology, 2002:1, pp. 31-37.

[5] This work has not yet been reported in a public forum. Patent applications have been submitted.

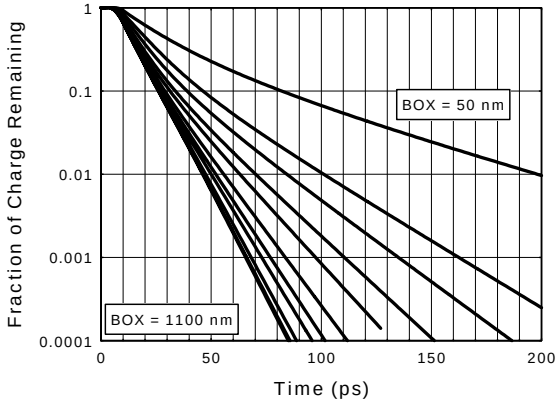

Figure 1. Fraction of charge remaining in the source well of a CCD during transfer to the next well. The speed improves dramatically as the BOX thickness increases.

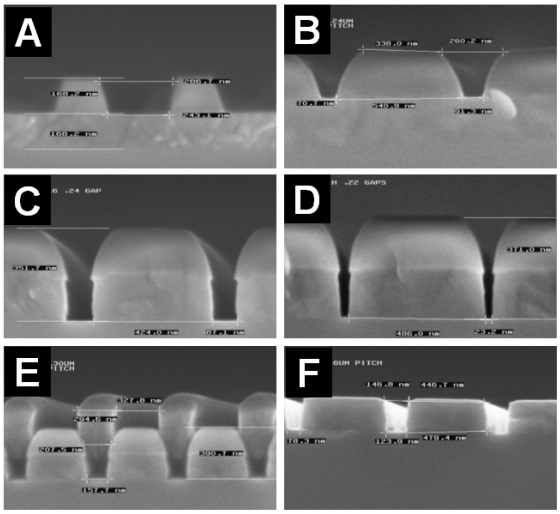

Figure 2. Series of SEM images showing the steps in the fabrication of narrow gaps within a single layer of polysilicon gate material.

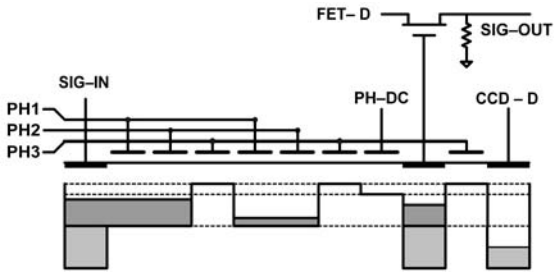

Figure 3. The top part shows a schematic view of a two-stage CCD shift register and the on-chip source follower output amplifier. The potentials in the channel under the gates and the packets of charge in the CCD are illustrated in the lower part of the figure for the point in the clock sequence when a charge packet is in the output sensing diffusion.

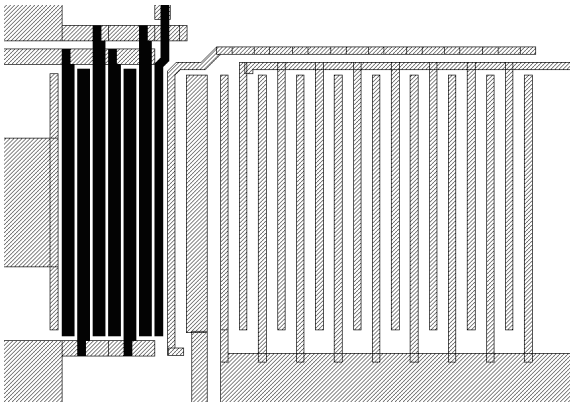

Figure 4. This is a captured image of the layout of a two-stage CCD, corresponding to the diagram in Fig. 3. The polysilicon gates are shown in solid black on the left. Metal wiring is shown in grey. The structure on the right is the large, interdigitated FET of the output amplifier. Only the metal lines that contact the source and drain are shown; its polysilicon gates, which are defined in a different drawing layer, have been suppressed.

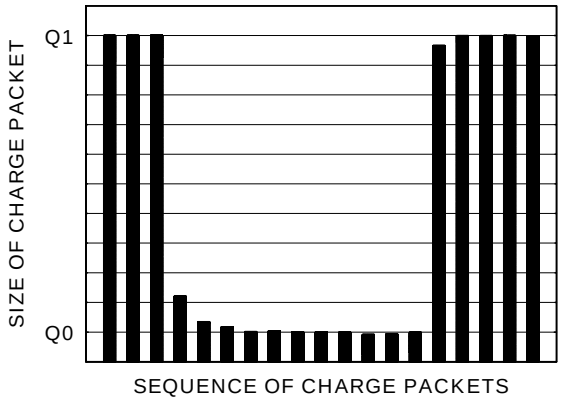

Figure 5. Sequence of charge packets read out from a 200-stage CCD shift register. The input packets formed a square pulse with small packets (Q0) and large packets (Q1). The rounding at the transitions is the result of imperfect charge transfer, estimated to be about 0.9995 per stage or 0.9998 per transfer.